Application No. 10/717,323
In Response to Office Action Mailed on June 1, 2006
Response Dated: July 26, 2006

LISTING OF THE (AMENDED) CLAIMS

1. (currently amended) A method of resynchronizing a clock signal to a data stream comprising:

receiving said clock signal by a first delay line, said clock signal having a frequency equivalent to one-half ~~a~~the frequency of said data stream;

receiving said clock signal by a second delay line;

generating a first delayed clock signal from said first delay line using a first control signal, said first control signal effecting a first delay such that said first delayed clock signal is characterized by a level transition aligned approximately at ~~a~~the midpoint of a valid data period of said data stream;

generating a second delayed clock signal from said second delay line using a second control signal, said second control signal used to effect a second delay to said second delayed clock signal;

clocking said data stream using a first pair of first digital logic devices to generate a first data sequence, said clocking performed using said first delayed clock signal;

clocking said data stream using a second pair of first digital logic devices to generate a second data sequence, said clocking performed using said second delayed clock signal;

generating an output based on said first data sequence and said second data sequence;

clocking said output using a second digital logic device to generate an indicator, said clocking performed by said first delayed clock signal; and

evaluating said indicator.

2. (original) The method of Claim 1 wherein said first digital logic device comprises flip-flops and registers.

PAGE 4/14 * RCVD AT 7/26/2006 5:44:53 PM [Eastern Daylight Time] * SVR:USPTO-EFXRF-1/15 * DNIS:2738300 * CSID:3127079155 * DURATION (mm-ss):03-46

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3. (original) The method of Claim 1 wherein said first digital logic device comprises registers.

4. (original) The method of Claim 1 wherein said second digital logic device comprises a flip-flop.

5. (original) The method of Claim 1 wherein said second delay is such that the sequence of bits provided by first data sequence is equivalent to the sequence of bits provided by said second data sequence.

6. (original) The method of Claim 1 wherein generating an output based on said first data sequence and said second data sequence comprises applying a function to said first data sequence and said second data sequence, and wherein said function is implemented by using of one or more EXCLUSIVE NOR gates connected to one or more AND gates.

7. (original) The method of Claim 1 wherein said first pair of first digital logic devices is used to concatenate a portion of said first data sequence to a remaining portion of said first data sequence during a single period of said first delayed clock signal.

8. (original) The method of Claim 7 wherein a first flip-flop or register of said first pair of first digital logic devices is sampled by a positive level transition of said first delayed clock signal and a second register of said first pair of first digital logic devices is sampled by a negative level transition of said first delayed clock signal.

9. (original) The method of Claim 7 wherein a first flip-flop or register of said first pair of first digital logic devices is sampled by a negative level transition of said first delayed clock signal and a second register of said first pair of first digital logic devices is sampled by a positive level transition of said first delayed clock signal.

10. (original) The method of Claim 8 wherein said second pair of first digital logic devices is used to concatenate a portion of said second data sequence to a remaining portion of said second data sequence during a single period of said second delayed clock signal.

PAGE 5/14 * RCVD AT 7/26/2006 5:44:53 PM [Eastern Daylight Time] * SVR:USPTO-EFXRF-1/15 * DNIS:2738300 * CSID:3127079155 * DURATION (mm-ss):03-46

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11. (original) The method of Claim 10 wherein a first flip-flop or register of said second pair of first digital logic devices is sampled by a positive level transition of said second delayed clock signal and a second register of said second pair of first digital logic devices is sampled by a negative level transition of said second delayed clock signal.

12. (original) The method of Claim 10 wherein a first flip-flop or register of said second pair of first digital logic devices is sampled by a negative level transition of said second delayed clock signal and a second register of said second pair of first digital logic devices is sampled by a positive level transition of said second delayed clock signal.

13. (original) The method of Claim 1 wherein a logical value of said indicator is used to indicate whether said second delay of said second delayed clock signal is within an acceptable range.

14. (original) The method of Claim 1 further comprising tabulating said output using a software program stored in a memory and executed by a processor.

15. (original) The method of Claim 1 further comprising incrementing or decrementing said second delay by way of said second control signal in order to establish an acceptable range of said second delay.

16. (original) The method of Claim 15 wherein said incrementing or decrementing is performed by way of a software program executed by a processor.

17. (original) The method of Claim 15 wherein said acceptable range is used to determine a median or average value of said second delay.

18. (original) The method of Claim 17 wherein said median or average delay value is used to adjust or correct said first delay used in said first delay line.

19. (currently amended) A system for resynchronizing a clock signal to a data stream over a data interface comprising:

PAGE 6/14 * RCVD AT 7/26/2006 5:44:53 PM [Eastern Daylight Time] * SVR:USPTO-EFXRF-1/15 * DNIS:2738300 * CSID:3127079155 * DURATION (mm-ss):03-46

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a first delay line outputting a first delayed clock signal, said first delay line capable of receiving a first control signal, said first control signal effecting a first delay such that said first delayed clock signal is characterized by a level transition aligned approximately at ~~a~~the midpoint of a valid data period of said data stream;

a second delay line outputting a second delayed clock signal, said second delay line capable of receiving a second control signal, said second control signal used to effect a second delay to said second delayed clock signal;

a first pair of registers used to generate a first data sequence, said first pair of registers clocked by said first delayed clock signal;

a second pair of registers used to generate a second data sequence, said second pair of registers clocked by said second delayed clock signal;

a digital logic circuit used to apply a function to said first data sequence and said second data sequence; and

a digital logic device configured to generate an indicator signal, said digital logic device clocked by said first delayed clock signal.

20. (original) The system of Claim 19 further comprising:

a memory;

a set of software instructions resident in said memory;

a processor used to execute said software instructions; and

a user interface used to provide control of said processor.

21. (original) The system of Claim 19 further comprising a hardwired or microprogrammed state machine.

PAGE 7/14 * RCVD AT 7/26/2006 5:44:53 PM [Eastern Daylight Time] * SVR:USPTO-EFXRF-1/15 * DNIS:2738300 * CSID:3127079155 * DURATION (mm-ss):03-46

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22. (original) The system of Claim 19 wherein said digital logic circuit comprises one or more AND gates connected to one or more EXCLUSIVE NOR gates.

23. (original) The system of Claim 19 wherein said digital logic device comprises a flip-flop.

24. (original) The system of Claim 19 wherein said digital logic device comprises a register.

25. (original) The system of Claim 19 wherein said indicator is used to establish an acceptable range for said second delay.

26. (original) The system of Claim 25 wherein said acceptable range is used to determine a median or average value of said second delay.

27. (original) The system of Claim 26 wherein said median or average delay value is used to adjust or correct said first delay.

28. (original) The system of Claim 26 wherein said median or average value of said second delay is used to re-align said level transition of said valid data period of said data stream.

29. (original) The system of Claim 19 wherein said data interface comprises a DDR interface within an ASIC device.

30. (original) The system of Claim 19 wherein said data interface comprises a DDR interface within a DRAM device.

31. (original) The system of Claim 19 wherein said data interface comprises a SDRAM interface within an ASIC device.

32. (original) The system of Claim 19 wherein said data interface comprises a SDRAM interface within a DRAM device.

33. (original) The system of Claim 19 wherein said data interface comprises a SER-DES interface.

PAGE 8/14 * RCVD AT 7/26/2006 5:44:53 PM [Eastern Daylight Time] * SVR:USPTO-EFXRF-1/15 * DNIS:2738300 * CSID:3127079155 * DURATION (mm-ss):03-46

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34. (original) The system of Claim 19 wherein said data interface comprises a SATA interface.

35. (original) The system of Claim 19 wherein said data interface comprises a USB interface.

36. (original) The system of Claim 19 wherein said data interface comprises a IEEE 1394 interface.

37. (original) The system of Claim 19 wherein said data interface comprises a quad data rate interface.

38. (original) The system of Claim 19 wherein said data interface comprises an octal data rate interface.

39. (original) The system of Claim 19 wherein said first delay line or second delay line comprises a selectable delay line.

40. (original) The system of Claim 39 wherein said first delay line or said second delay line comprises a numerically controlled delay line.

41. (original) The system of Claim 39 wherein said first delay line or said second delay line comprises a voltage controlled delay line.

42. (currently amended) A system for resynchronizing a clock signal to a data stream comprising:

a first delay line capable of receiving a first control signal, said first control signal effecting a first delay to a first delayed clock signal such that said first delayed clock signal is characterized by a level transition aligned approximately at ~~athe~~ midpoint of a valid data period of said data stream;

a second delay line capable of receiving a second control signal, said second control signal used to effect a second delay to a second delayed clock signal;

PAGE 9/14 * RCVD AT 7/26/2006 5:44:53 PM [Eastern Daylight Time] * SVR:USPTO-EFXRF-1/15 * DNIS:2738300 * CSID:3127079155 * DURATION (mm-ss):03-46

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a first pair of first digital logic devices used to generate a first data sequence, said first pair of first digital logic devices capable of concatenating a portion of said first data sequence to a remaining portion of said first data sequence during a single period of said first delayed clock signal;

a second pair of first digital logic devices used to generate a first data sequence, said second pair of first digital logic devices capable of concatenating a portion of said second data sequence to a remaining portion of said second data sequence during a single period of said second delayed clock signal;

a circuitry used to apply a function to said first data sequence and said second data sequence;

a flip-flop or register configured to generate an indicator signal, said flip-flop or register clocked by said first delayed clock signal.

PAGE 10/14 * RCVD AT 7/26/2006 5:44:53 PM [Eastern Daylight Time] * SVR:USPTO-EFXRF-1/15 * DNIS:2738300 * CSID:3127079155 * DURATION (mm-ss):03-46

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